Electronic Version
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Claims

[c1] 1. A memory architecture used to repair a serial access memory comprising a main memory, a redundant memory and a control interface circuit, the control interface circuit storing a plurality of addresses, each of the addresses corresponding to a damaged memory cell in the main memory,
when the memory module is accessed by an access address, the control interface circuit issuing a pointer address pointing to a corresponding address in the stored addresses in the control interface circuit and comparing the address corresponding to the pointer address and the access address. If the address corresponding to the pointer address is equal to the access address, data accessed by the access address from the memory module is read out from the redundant memory.

[c2] 2. The memory architecture of claim 1, the data accessed by the access address from the memory module being read out from a memory address of the redundant memory, the memory address corresponding to the pointer address issued by the control interface circuit.

[c3] 3. The memory architecture of claim 1, each of the ad-

dresses stored in the control interface circuit having a memory address that corresponds to the redundant memory, if the address corresponding to the pointer address is equal to the access address, the data read out from the memory address of the redundant memory corresponds to the address.

[c4] 4. The memory architecture of claim 1, the control interface circuit comprising:
a pointer control unit coupled to the redundant memory, that generates the pointer address;
a fuse box, coupled to the pointer control unit registering the addresses of the damaged cells of the main memory and outputting one of the addresses according to the pointer address;
a comparable logic unit, coupled to the fuse box comparing the access address with the address output from the fuse box, and generating a redundant selection signal if the address corresponding to the pointer address is equal to the access address,
if the redundant selection signal being activated, the data accessed by the access address from the memory module being read out from the redundant memory.

[c5] 5. The memory architecture of claim 4, the control interface circuit comprising a data selection unit, coupled to the application circuit, the main memory, the redundant

memory, the comparable logic unit,
if the redundant selection signal being activated, the data accessed by the access address from the memory module being read out from the redundant memory,
if the redundant selection signal being not activated, the data accessed by the access address from the memory module being read out from the main memory.

[c6] 6. The memory architecture of claim 5, wherein the data selection unit includes a multiplexing circuit.

[c7] 7. The memory architecture of claim 4, wherein the comparable logic unit includes an assembly of NOR gates.

[c8] 8. The memory architecture of claim 4, wherein the pointer control unit increments the pointer address by a step value when the redundant selection signal is set.

[c9] 9. The memory architecture of claim 8, wherein the step value is one.

[c10] 10. The memory architecture of claim 4, wherein the pointer control unit decrements the pointer address by a step value when the redundant selection signal is set.

[c11] 11. The memory architecture of claim 8, wherein the step value is one.

[c12] 12. The memory architecture of claim 4, wherein the

fuse box registers the addresses of the damaged cells of the main memory by cutting off a plurality of fuses in the fuse box by using a laser.

[c13] 13. The memory architecture of claim 1, wherein the main memory is a first-in-first-out memory circuit.

[c14] 14. A method for repairing a serial access memory, the memory module comprising a main memory, a redundant memory and a control interface circuit, the control interface circuit for storing a plurality of addresses, each of the addresses corresponding to a damaged memory cell in the main memory,
assessing the memory module by an access address;
issuing a pointer address by the control interface circuit to point to a corresponding one of the stored addresses stored in the control interface circuit;
comparing the address corresponding to the pointer address and the access address, if the address corresponding to the pointer address is equal to the access address, data accessed by the access address from the memory module being read out from the redundant memory.

[c15] 15. The method of claim 14, wherein the memory address corresponds to the pointer address issued by the control interface circuit.

[c16] 16. The method of claim 14, wherein
if the redundant selection signal is activated, the data accessed by the access address from the memory module is read out from the redundant memory,
if the redundant selection signal being not activated, the data accessed by the access address from the memory module is read out from the main memory.

[c17] 17. The method of claim 14, wherein the pointer address is incremented by a step value when the redundant selection signal is set.

[c18] 18. The method of claim 17, wherein the step value is one.

[c19] 19. The method of claim 14, wherein the pointer address is decremented by a step value when the redundant selection signal is set.

[c20] 20. The method of claim 19, wherein the step value is one.

[c21] 21. The method of claim 14, wherein the main memory is a first-in-first-out memory circuit.